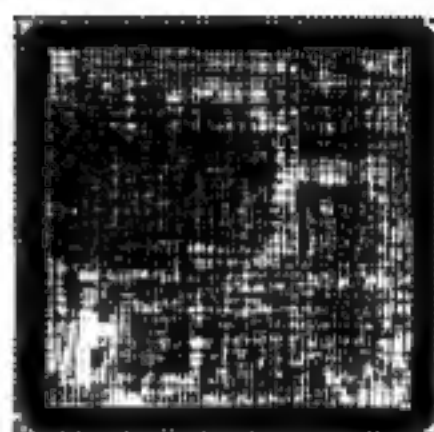
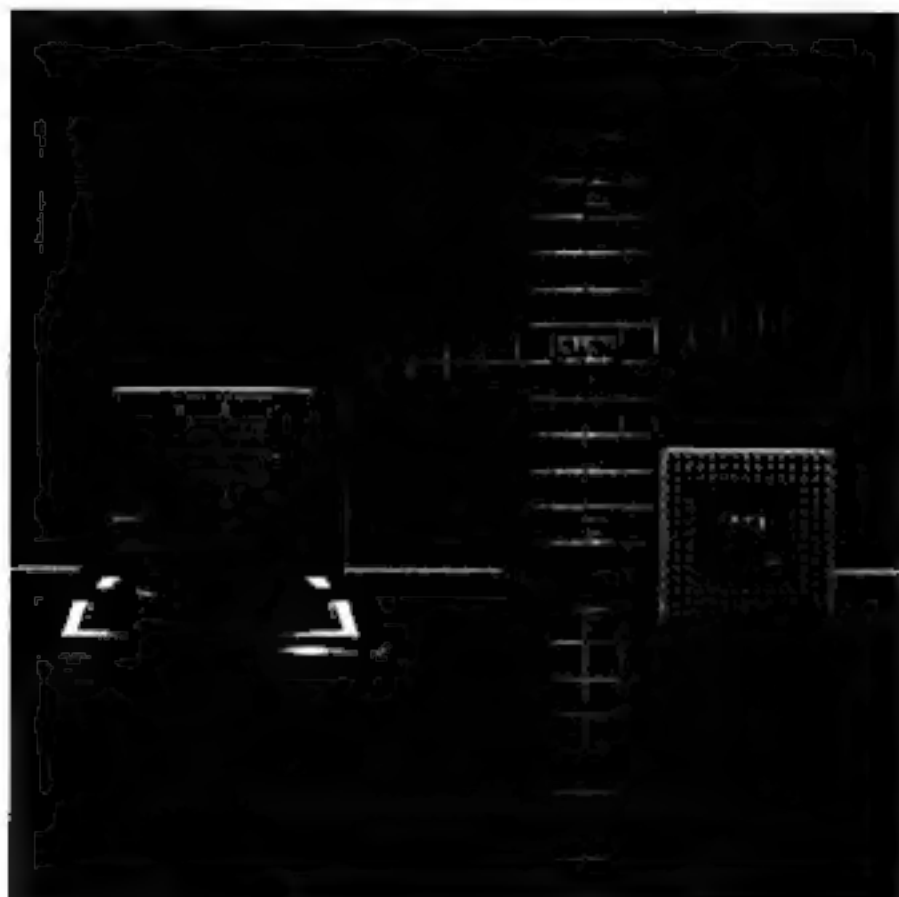


## Semicustom ICs



### SCxE6: »Sea-of-Gates« Gate-Arrays

Siemens announces  
a sub-micron generation  
of channelless gate-arrays  
based on the proven  
Megalogic process

#### Features

- Advanced 0.8 micron (drawn gate-length) ACMOS5H Megalogic technology
- 0.28 ns speed (2 input NAND, fanout = 2)
- Slew rate control option
- High packing density featuring over 300,000 available gates
- Full workstation support (e.g. Cadence, Mentor, Valid, Dasix)
- Reduced design turnaround time due to cell preplacement and delay calculation
- Fully hierarchical design flow capability
- Alternately sourced by Toshiba

### SCxE6: Sub-Micron ASICs »Made in Europe«

Continuing development of the proven Megalogic process now enables Siemens to offer their proven channelless gate-array architecture with sub-micron transistors.

Offering a 30% speed improvement over its 1 micron predecessor, the SCxE6 family's enhanced packing density, coupled with the new Siemens Logic Design System CAD tools, offers the gate-array performance needed to revolutionize your system design.

All **»Made in Europe«** of course!

# SCxE6 Electrical Characteristics

## Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
DC supply voltage	$V_{DD}$	-0.3 ... 7.0	V
Input voltage	$V_I$	-0.3 ... $V_{DD} + 0.3$	V
Output voltage	$V_O$	-0.3 ... $V_{DD} + 0.3$	V
DC input diode current	$I_{IH}$	-20 ... 20	mA
DC output diode current	$I_{OL}$	-20 ... 20	mA
Storage temperature	$T_{STB}$	-85 ... 150	°C
Junction temperature (during operation)	$T_J$	150	°C

(1) See table DC specification I/O cells in data sheets

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
DC Supply Voltage ( $V_{DD} = 0V$ )	$V_{DD}$	4.5	5.5	V
Input voltage	$V_I$	0	$V_{DD}$	V
Output voltage	$V_O$	0	$V_{DD}$	V
Input rise and fall times	$t_{in}, t_f$	0	5	ns
Junction temperature (2)	$T_J$	0	125	°C

(1) Functional range of inputs with CMOS-compatible inputs is 2.0 ... 6.0V

(2) Extended temperature range on request

## Macro Cells

### High Speed ROM / Low Power ROM

- Configuration: 64 - 1024 words; 2 - 32 bit
- Capacity: max. 16 Kbit/Block
- Read Access Time: 10/14 ns typical

### Single Port RAM

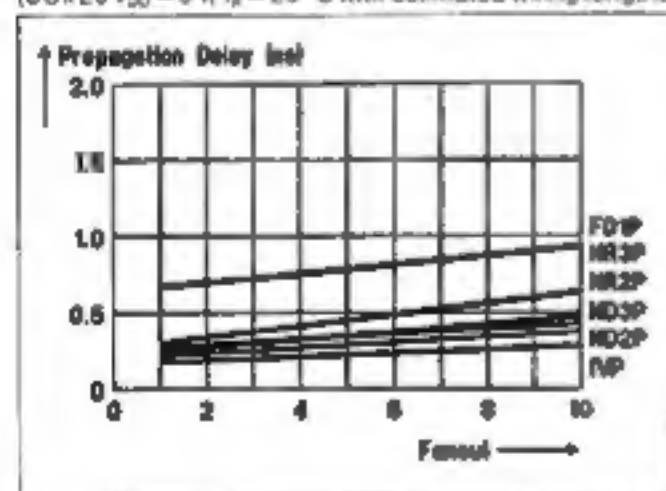
- Configuration: 8 - 256 words; 4 - 36 bit
- Capacity: max. 4.5 Kbit/Block
- Read Access Time: 6 ns typical

### Triple Port RAM

- Configuration: 16 - 64 words; 4 - 36 bit
- Capacity: max. 2.3 Kbit/Block
- Read Access Time: 5 ns typical

## Basic Cell Delay vs Fanout

(SCxE6  $V_{DD} = 5V$ ,  $T_A = 25^\circ C$  with estimated wiring lengths)



# SCxE6 Series Design Flow

T-42-11-09

## Design Automation - The Key to Success

The SCxE6 gate-array family is fully supported by ADVANCAD, a highly sophisticated CAD system for the development of VLSI ASICs. ADVANCAD is based on industry standard software packages supplemented with the Siemens Logic Design System (SLDS), available for use on popular engineering workstations.

## SLDS - Workstation Support

The Siemens Logic Design System (SLDS), used in conjunction with industry standard workstation CAD packages, offers the user an ASIC design system without parallel. Powerful enough to permit cell preplacement, accurate enough to correctly calculate the effects of parasitic wiring capacitance, even before netlist transfer to the "back-end" design environment. This may reduce the turnaround time of your design significantly. And flexible enough to interface to your existing CAD environment!

## Customer Interfaces

Customer develops up to the interface shown			
Development steps	Customer develops the logic diagram	Customer with workstation	Customer with workstation and own CAD-system, also silicon foundry
• Product idea/circuit design			
• Conversion of circuit into logic diagram by using design manual and cell library			
• Logic entry			
• Logic simulation			
• Layout generation			
• Logic simulation including wiring delays			
• Approval of simulation results			
• Testprogram generation			
• Tape for mask generation			
• Water fabrication			
• Wafer test			
• Assembly			
• Testing			
• Samples			

responsibility of Siemens  
responsibility of customer

## Available Masters

Part Number	Gate <sup>(1)</sup> Complexity	Estimated <sup>(2)</sup> Usable Gates	Maximum Pads <sup>(3)</sup>	max I/O Pads <sup>(4)</sup>
SC33 E8	33000	13000	158	144
SC41 E8	41000	17000	174	160
SC54 E8	54000	22000	198	184
SC70 E8	70000	28000	222	208
SC108 E8	108000	43000	270	256
SC132 E8	132000	63000	294	280 (256)
SC177 E8	177000	71000	334	320 (256)
SC235 E8	235000	94000	382	368 (256)
SC302 E8	302000	120000	430	416 (256)

Notes: 1. Row-gate. 2. Based on 40 % array utilization. Actual utilization varies, depending on cell types used.

3. Additional I/O pads may be configured as V<sub>DD</sub>/V<sub>SS</sub>, subject to number and drive of output buffers. 4. Tester limitation of 25 k I/O.

## Standard Packaging Spectrum

Master	SC33 E8	SC41 E8	SC54 E8	SC70 E8	SC108 E8	SC132 E8	SC177 E8	SC235 E8	SC302 E8
Max I/O Pads	144	160	184	208	256	280	320	368	416
P-LCC-28	+								
P-LCC-44	+	+	+	+					
P-LCC-68	+	+	+	+	+	+			
P-LCC-84	+	+	+	+	+	or			
P-MQFP-80	+	+	+	or					
P-MQFP-100	+	+	+	+					
P-MQFP-144	+	+	+	+	+	+	+		
P-MQFP-160		+	+	+	+	+	+		
P-MQFP-208					+	+	+	□	
P-MQFP-240					or	or	or	or	or
P-MQFP-304					or	or	or	or	or
M-QUAD-160*)	or	or	or	or	or	or	or	or	or
M-QUAD-208*)				or	or	or	or	or	or
M-QUAD-240*)					or	or	or	or	or
M-QUAD-304*)							or	or	or
C-PGA-84-D	+	+	+	+					
C-PGA-72-D	+	+	+	+	+				
C-PGA-88-D	+	+	+	+	or	or	+	+	
C-PGA-120-D	+	+	+	+	+	+			
C-PGA-132-D	+	+	+	+	or	or			
C-PGA-144-D				+	+	+			
C-PGA-223-D				+	+	+	or	+	+
C-PGA-298-D				or	or	or	or	+	+
C-PGA-381-D								or	or
C-PGA-144-U	+	+	+	+					
C-PGA-179-U			+	+	+	+	+		
C-PGA-224-U				+	+	+			

+ = available; □ = in preparation; or = on request; U = cavity up; D = cavity down.

\*) M-QUAD is a trademark owned by Dln.

Please enquire for any type not shown.

## Worldwide Design Support

Design Centres:

Munich  
Stuttgart  
Mannheim  
Düsseldorf

Milan  
London\*  
Zurich\*  
Santa Clara

## Additional information available:

SCx E6 cell catalogue  
SLDS manual  
Packaging catalogue